

WHAT IS CLAIMED IS:

- 1 1. A photodiode comprising:  
2 a well located in a substrate;  
3 a floating node located in the well;  
4 shallow trench isolation (STI) regions located over and laterally opposing the  
5 floating node;  
6 a borderless contact buffer layer located over at least the floating node;  
7 a dielectric layer located over the borderless contact buffer layer; and  
8 a borderless contact extending through the dielectric layer and the borderless  
9 contact buffer layer to the floating node.
- 1 2. The photodiode of Claim 1 wherein the borderless contact buffer layer is selected  
2 from the group consisting of: SiON, SiN, and combinations thereof.
- 1 3. The photodiode of Claim 1 wherein the dielectric layer is selected from the group  
2 consisting of: silicon dioxide, low dielectric material, and combinations thereof.
- 1 4. The photodiode of Claim 1 wherein a second refractive index of the borderless  
2 contact buffer layer is between a first refractive index of the dielectric layer and a third  
3 refractive index of the floating node.
- 1 5. The photodiode of Claim 1 wherein the dielectric layer has a first refractive index  
2 of between about 1.3 and about 1.5, the borderless contact buffer layer has a second

3 refractive index of between about 1.8 and about 2.5, and the floating node has a third  
4 refractive index of greater than about 3.

1 6. The photodiode of Claim 1 wherein the well is doped with an n-type impurity and  
2 the floating node is doped with an n<sup>+</sup> type impurity.

1 7. A method of manufacturing a photodiode sensor, comprising:  
2 forming a well in a substrate;  
3 forming a shallow trench isolation (STI) element at least partially in the well;  
4 removing a portion of the STI element to form STI regions opposing an exposed  
5 portion of the well;  
6 forming a floating node in the exposed portion of the well;  
7 forming a borderless contact buffer layer over at least the floating node and along  
8 sidewalls of the STI regions;  
9 forming an interlevel dielectric layer over the borderless contact buffer layer; and  
10 forming a borderless contact extending through the interlevel dielectric layer and  
11 the borderless contact buffer layer to the floating node.

1 8. The method of Claim 7 wherein the borderless contact buffer layer is selected  
2 from the group consisting of: SiON, SiN, and combinations thereof.

1 9. The method of Claim 7 wherein the dielectric layer is selected from the group  
2 consisting of: silicon dioxide, low dielectric material, and combinations thereof.

1 10. The method of Claim 7 wherein a second refractive index of the borderless  
2 contact buffer layer is between a first refractive index of the dielectric layer and a third  
3 refractive index of the floating node.

1 11. The method of Claim 7 wherein the dielectric layer has a first refractive index of  
2 between about 1.3 and about 1.5, the borderless contact buffer layer has a second

3 refractive index of between about 1.8 and about 2.5, and the floating node has a third  
4 refractive index of greater than about 3.

1 12. The method of Claim 7 wherein the well is doped with an n-type impurity and the  
2 floating node is doped with an n+ type impurity.

1 13. The method of Claim 7 wherein the floating node is formed by implanting ions  
2 through an opening between the opposing STI regions.

1 14. The method of Claim 7 wherein the portion of the STI element is removed by a  
2 dry etching process.

1 15. The method of Claim 7 further comprising forming a conductive interconnect on  
2 the dielectric layer and contacting the borderless contact.

1     16.     A semiconductor device, comprising:  
2             first and second adjacent wells located in a substrate;  
3             a first transistor gate structure located over at least a portion of the first well;  
4             a floating node located in the second well;  
5             shallow trench isolation (STI) regions located over and laterally opposing the  
6     floating node;  
7             a borderless contact buffer layer located over at least the floating node and the  
8     first transistor gate structure;  
9             a dielectric layer located over the borderless contact buffer layer;  
10            a first borderless contact extending through the dielectric layer and the borderless  
11   contact buffer layer to the floating node;  
12            a second borderless contact extending through the dielectric layer and the  
13   borderless contact buffer layer to the first transistor gate structure; and  
14            an interconnect located over the dielectric layer and coupling the first and second  
15   borderless contacts.

1     17.     The device of Claim 16 wherein the borderless contact buffer layer is selected  
2     from the group consisting of: SiON, SiN, and combinations thereof.

1     18.     The device of Claim 16 wherein the dielectric layer is selected from the group  
2     consisting of: silicon dioxide, low dielectric material, and combinations thereof.

1     19.     The device of Claim 16 wherein a second refractive index of the borderless  
2     contact buffer layer is between a first refractive index of the dielectric layer and a third  
3     refractive index of the floating node.

1    20.    The device of Claim 16 wherein the dielectric layer has a first refractive index of  
2    between about 1.3 and about 1.5, the borderless contact buffer layer has a second  
3    refractive index of between about 1.8 and about 2.5, and the floating node has a third  
4    refractive index of greater than about 3.

1    21.    The device of Claim 16 wherein the second well is doped with an n-type impurity  
2    and the floating node is doped with an n+ type impurity.

1    22.    The device of Claim 16 wherein the first well is doped with a first impurity type  
2    and the second well is doped with a second impurity type opposite to the first impurity  
3    type.

1    23.    The device of Claim 16 further comprising: a third well doped with the first  
2    impurity type and located adjacent the second well on a side opposite the first well; and a  
3    second transistor gate structure located over portions of the second and third wells.